translation of DE 199 33 564.8

GR 99 P 2315

Description

Method for producing a vertical semiconductor transistor component and a vertical semiconductor transistor component

The invention relates to a method for producing a vertical semiconductor transistor component and to a vertical semiconductor transistor component of this type.

The ongoing increase in the packing density of circuits on semiconductor chips is placing ever greater demands on the process and circuit technology. Until now, planar MOS semiconductor components have been scaled by improvements in optical lithography systems. The shortening of the channel length of the transistors which this involves has at the same time the effect of enhancing performance. With a further reduction in the structure sizes, however, two main problems arise.

Firstly, the concept of the planar "bulk" MOSFET (metal-oxide-semiconductor field-effect transistor) reaches its limit, since parasitic short-channel effects reduce the performance capability of this component. In this context, it has already been attempted to counteract the loss in performance by technologically complex channel doping profiles ("pockets" or "retrograde wells"). Further concepts currently being pursued to avoid parasitic short-channel effects comprise the production of transistors on SOI (Silicon-on-Insulator) wafers or the development of planar dual-gate transistors, in which improved gate control is achieved by embedding the channel region between two opposing gate electrodes.

The other problem is that the optical lithography systems are likely to reach their performance limits before long. An alternative scaling possibility is

provided by the concept of vertical components (in contrast to

planar components). With a vertical type of construction, channel lengths of below 100 nm can be readily achieved in the case of MOSFETs, since the channel length can be set with great accuracy by prescribing a layer thickness.

In German Patent Application DE 196 32 835 A1 there is a description of a semiconductor capacitor which has a capacitor electrode with vertical pillar structures to enlarge its capacitor area. The pillar structures are formed using a random mask, which permits structure sizes in the sub-100 nm range.

In the publication "Self-limiting oxidation for fabricating sub-5 nm silicon nanowires" by H.I. Liu, et al., "Appl. Phys. Lett." 64 (11), pages 1383-1385 (1994), a description is given of a lateral oxidation process, with which it is possible to produce vertical 2 nm wide silicon pillar structures which are surrounded by an SiO_2 sheath.

In the publication "Fabrication of silicon nanopillars containing polycrystalline silicon/insulator multilayer structures", by H. Fukuda, et al., "Appl. Phys. Lett." 70 (3), pages 333-335 (1997), a single-electron transistor is proposed, which comprises silicon pillar structures which are produced by the lateral oxidation method described in the publication mentioned above and which, furthermore, contain a plurality of tunnel isolation layers oriented in the transverse direction with respect to the pillar axis.

The invention is based on the object of specifying a method for producing a vertical semiconductor transistor component which makes it possible for powerful and scalable components of this type to be produced. The invention is also aimed at providing semiconductor transistor components which are powerful,

in particular have a high current driver capacity, and can be scaled.

The object on which the invention is based is achieved by the features of claims 1 and 8.

Accordingly, the channel length of the vertical semiconductor transistor component according to the invention is defined by a layer-producing step, while the channel width is fixed independently of the lithography by a random mask. In this case, the "channel" of the vertical semiconductor transistor component is represented by a plurality of individual channels, which are formed in the pillar structures and have the same length and substantially the same width. The combination of these two principles (definition of all the individual channel lengths by a common layer-producing step and definition of the individual channel widths by a random mask) makes it possible to produce a short-channel FET with small individual channel widths and also makes possible a substantially complete punchthrough of the potential generated by the second electrical contact (gate) through the individual channels, whereby effective transistor control is made possible and parasitic short-channel effects are eliminated. The number of pillar structures comprised by the component can in this case be verified by the mask forming process (and a following lithographic selection step) and set according to the conditions and practical requirements, in particular with regard to the desired performance characteristics of the transistor.

The series of layers is preferably built up by a selective n^+pn^+ or p^+np^+ epitaxial step. It is possible by suitable doping to compensate for moderate fluctuations in the pillar structure diameters (for example 50 nm ± 10 nm) and achieve the effect that the lowly doped middle layer zones (channel layer zones) of the pillar structures go over into the completely

depleted state when there is a corresponding gate voltage.

In an alternative way, the series of layers may also be built up by a deposition of alternating semiconductor layers and tunnel isolation layers, the layer thickness of the tunnel isolation layers being less than 5 nm. In this way, a semiconductor transistor component based on the electrical tunnel effect is realized.

If the semiconductor layers consist of silicon, a further considerable reduction in the lateral dimensions of the silicon layer zones can be achieved after the pillar structures have been formed from the series of layers by a lateral oxidation step. The underlying principle is described in the publication cited at the beginning by H.I. Liu, et al., and leads to the result that silicon is retained only in a very thin core region (diameter approximately 2 nm) of the pillar structure, while the entire surrounding sheath region of the pillar structure is oxidized. The attainable restriction of charge carriers in all dimensions allows quantum components and single-electron components to be realized on a silicon base, the production of which requires only conventional process steps (depositing, etching and self-adjusting oxidation processes).

If a multiplicity of tunnel isolation layers are provided, MTJ (multiple tunnel junctions) can also be produced in particular.

Further advantageous refinements of the invention are specified in the subclaims.

The invention is explained in more detail below on the basis of two exemplary embodiments with reference to the drawing, in which:

figures 1A-P show schematic sectional representations to explain the process steps which are carried out for building up

a vertical FET according to the invention as in the case of a first exemplary embodiment of the invention;

figure 2A shows a schematic sectional representation of a vertical FET produced by the method explained in figures 1A-P;

figure 2B shows a representation in plan view of the vertical FET shown in figure 2A, the contours of lithographic masks used in the production being depicted;

figure 2C shows a schematic sectional representation aligned with figures 2A and 2B to illustrate the lithographic masks used;

figure 3 shows a schematic perspective view of a vertical FET according to the invention;

figure 4A shows a schematic sectional representation of a single pillar structure to realize a single-electron or quantum FET according to the invention as in the case of a second exemplary embodiment of the present invention; and

figure 4B shows the pillar structure represented in figure 4A after execution of a lateral self-restricting oxidation step.

According to figure 1A, a continuous conductive contact layer 2 is produced on a substrate 2, for example a monocrystalline silicon wafer. The conductive contact layer 2 may be, for example, a doped epitaxial layer or a doped surface region of the substrate 1.

A thermal oxide layer 3, for example 700 to 800 nm thick, is subsequently grown onto the contact layer

2. An active region 4 is etched free by means of a standard LOCOS mask L1 (LOCOS: LOCal Oxidation of Silicon), see figure 1B. The remaining oxide structures 3 serve for isolation with respect to neighboring transistor structures (not represented).

As an alternative to the LOCOS technique represented in figure 1B, the trench isolation technique (STI: shallow trench isolation) can also be used for the electrical isolation of neighboring transistor structures. In the case of this technique, narrow trenches are etched into the contact layer 2 and the substrate 1 and filled with an insulating material, a smaller space requirement being needed than in the case of the LOCOS isolating technique.

In a preferred selective epitaxial step (see figure 1C), a series of layers 5, 6, 7 is grown on in the exposed active region 4. On account of the selectivity of the epitaxial step, no mask is required for this. The layers 5, 6, 7 may be, for example, n^+-, p- and n^+-doped silicon layers or p^+-, n-, p^+-doped silicon layers. It is also possible to produce polycrystalline or possibly even amorphous doped silicon layers 5, 6, 7.

In a next step (see figure 1D), a capping isolation layer 8 is deposited over the series of layers 5, 6, 7 and the surrounding thermal oxide 3. The approximately 20 nm thick capping isolation layer 8 may be, for example, an SiO_2 layer and be deposited by the known TEOS (tetraethyl orthosilicate) method. The capping isolation layer 8 is used later as a hard-surface mask for forming the pillar structures.

A first possible way of producing a random mask is described in more detail with reference to the

following figures 1E to 1G. Randomly distributed mask structures

in the form of seeds 9 are formed on the surface of the capping isolation layer 8 during a vapor phase deposition in an epitaxial installation. An atmosphere comprising H_2 and SiH_4, with which GeH_4 is admixed to delay the nucleation process, is used as the process gas. The partial pressure of SiH_4 and GeH_4 lies in the range of 10^{-3} to 1 mbar, the partial pressure of H_2 may be approximately 1 to 100 mbar. The deposition is carried out in the temperature range between 500 - 700°C. Under these process conditions, individual silicon seeds are formed on the surface of the capping isolation layer 8 and determine the distribution and density of the randomly distributed mask structures. As soon as the density of the silicon seeds has reached a predetermined value, for example approximately 10^{10} to $10^{12}/cm^2$, the nucleation process is discontinued.

Subsequently, the process conditions are changed in order to set specifically the size of the silicon seeds. For this purpose, process conditions such as those used for selective epitaxy are set. Further nucleation on the surface of the capping isolation layer 8 is then prevented. The selective epitaxy takes place for example with a gas mixture of H_2 and SiH_2Cl_2 in the temperature range between 600 - 800°C. GeH_4 may be added to this gas mixture, in order to set the material composition of the seeds 9.

As soon as the diameter of the seeds 9 corresponds to a predetermined value, the depositing process is discontinued. The seeds 9 form randomly distributed mask structures of a random mask according to figure 1E.

A random mask can also be produced in a different way. Another possible way is to apply to the capping isolation layer 8 a continuous germanium layer, which disintegrates in a subsequent annealing step (for

example at 500°C) into individual germanium seeds, which form the randomly distributed mask structures.

A third possible way is to apply to the capping isolation layer 8 a layer with a deliberately rough surface. The layer may, for example, consist of polysilicon or polygermanium. With an average thickness of, for example, 50 nm, thickness fluctuations of the layer of 30 nm can be realized. Randomly distributed mask structures can be produced by an anisotropic etching process, by the surface of the capping isolation layer 8 being exposed earlier at locations of lesser thickness of the overlying layer with a rough surface than at locations of greater layer thickness.

According to a fourth possible method of producing a random mask, a first silicon layer of a thickness of 20 nm, for example, may be applied to the capping isolation layer 8, an SiO_2 layer of a thickness of 3 nm, for example, may be applied on top of that and a second silicon layer of a layer thickness of approximately 20 nm may be applied on top of that. In an annealing step at approximately 1000°C, the SiO_2 layer embedded between the silicon layers disintegrates and forms individual SiO_2 islands, which can be used as randomly distributed mask structures after removal of the upper silicon layer (and a structuring of the lower silicon layer occurring as this happens).

After the random mask has been formed, a component region is defined according to figure 1F by means of a selection mask L2, by unmasked seeds 9 being etched away. Masked seeds, on the other hand, remain. The selection mask step defines both the location of the component to be formed and the number of vertical pillar structures occurring in it.

In a next process step (figure 1G), the capping isolation layer 8 is removed by anisotropic etching. The random mask of seeds 10 is transferred into the

capping isolation layer 8, where it forms a hard-surface mask 11.

According to figures 1H and 1I, after this the series of layers 5, 6, 7 is etched using the seeds 10 or the hard-surface mask 11 and then the remains of the seeds 10 and of the hard-surface mask 11 are removed. In this operation, pillar structures 12 are formed from the series of layers 5, 6, 7. The pillar structures 12 comprise a series of layer zones 5A, 6A and 7A according to the original series of layers 5, 6, 7.

Subsequently, a thin isolation layer 13 is produced on the exposed wall regions of the pillar structures 12 and on the surface of the contact layer 2. The isolation layer 13 may comprise a 3 to 5 nm thick thermal SiO_2 layer, which is grown on at approximately 700 - 800°C, and which serves at the circumference of the pillar structures 12 as a gate oxide layer of the vertical transistor component to be produced (figure 1K).

Figure 1L illustrates the depositing of a layer 14 of in-situ-doped polysilicon (n^+ or p^+) over the structure shown in figure 1K. In this case, the previously existing free regions between the pillar structures 12 are filled by the polysilicon (known as "gate filling").

In a further step, the gate electrode (second contact) of the transistor component to be produced is formed by means of a gate definition mask L3. For this purpose, the polysilicon is etched back by a certain amount in the regions not covered by the gate definition mask L3. The gate definition mask L3 is oriented here in such a way that it at least partially covers at least some pillar structures 12 lying at the edge of the component region defined by the selection mask L2, i.e. has a certain overlap with the selection mask L2 (see also figure 2C). The process parameters of the etching step are set in such a way that the polysilicon layer 14 is

reduced by its layer thickness, i.e. the filling height between the

pillar structures 12 is reduced approximately by the layer thickness and the level polysilicon layer 14 is completely removed in unmasked regions. The polysilicon layer 14 A structured in this way is shown in figure 1M.

In a following optional process step, an As dopant implantation is carried out (see figure 1N). The As dopant implantation can take place over the entire surface area, increases the conductivity of the gate polysilicon 14 and leads into a region alongside the pillar structures 12 to the formation of an n-doped well region 15 in the contact layer 2.

Figure 10 shows in a cross-sectional representation the situation after the depositing of an approximately 500 nm thick intermediate oxide layer 16 and a subsequently carried-out RTA (rapid thermal annealing) step, in which the intermediate oxide layer 16 is made to flow slightly by brief heat exposure, with the effect of rounding its contour. On account of the short duration of the heat exposure, the occurrence of undesired diffusion processes can be largely prevented here.

In a further mask step, contact holes K1, K2 and K3 are introduced into the intermediate oxide layer 16 by means of a contact hole mask L4. The contact hole L1 is located above the well region 15 and serves for the electrical bonding of the bases of the pillar structures 12. The contact hole K2 permits the electrical bonding of the polysilicon layer structure 14A. The contact hole K3 is located directly above the pillar structures 12 and permits electrical bonding of the same on the capping side.

In a final process step (see figure 1P), a contact metal is deposited in the bonding holes K1, K2 and K3

and structured by means of a metallization mask L5. The metal traces (see figure 2C) structured by the metallization mask L5 are larger than the corresponding

contact hole openings of the contact hole mask L4 and cover them. Figure 2A shows the finished vertical semiconductor transistor component. The contact material 17.1 filling the contact hole K1 realizes the source contact, the contact material 17.2 filling the contact hole K2 realizes the gate contact and the contact material 17.3 filling the contact hole K3 realizes the drain contact of the vertical MOSFET created.

Figure 2B shows the processing regions defined by the masks L1 to L5 in plan view. Here, the thicknesses (diameters) of the pillar structures 12 which lie within the component region defined by the selection mask L2 have been exaggerated for illustration reasons.

The method explained has the advantage that only conventional process steps are required. It is not restricted to silicon components, but may also be used in an analogous way for SiGe, SiC and for III-V semiconductor components. On account of the flexible design with respect to the number, thickness and densities of the pillar structures 12 contained in the component, both power transistors and logic transistors can be produced. The lithography-independent depositing and etching processes taking place in conjunction with the random mask achieve the effect that the transistor component remains scalable in spite of structure sizes in the sub-100 nm range.

Figure 3 shows the MOS semiconductor transistor component represented in figure 2A in a partly cut-open perspective view. It is clear that the polysilicon of the gate electrode 14A surrounds the pillar structures 12 on all sides at the height of the low-doped layer zone 6A.

By the modification to be described below, the method according to the invention also permits the production of single-electron or quantum components. The process

sequence explained in figures 1A - P is in this case initially modified to the extent that the series of layers 5, 6, 7 represented in figure 1C is now built up from alternately arranged silicon layers and tunnel isolation layers. Figure 4A shows the construction of a pillar structure 12', which is then formed in a way corresponding to the previous description from the modified series of layers. Tunnel isolation layer zones are designated by 6A' and silicon layer zones are designated by 5A'. The tunnel isolation layer zones 6A' may consist for example of Si_3N_4 and preferably have a layer thickness of approximately 1-2 nm. The layer thickness of the silicon layer zones 5A' (which may consist of crystalline silicon, polysilicon or amorphous silicon) may be approximately 10 to 20 nm. The diameter of the pillar structures 12' lies for example in the range of 50 to 150 nm and consequently corresponds to the diameter of the pillar structures 12 described in figures 1 to 3.

In a subsequent lateral, self-restricting oxidation step, the pillar structure 12' is oxidized in a foot and sheath region 13' by a dry oxidation process at temperatures in the range of 800 to approximately 1000°C over a period of approximately half an hour. On the basis of a self-restricting effect, which is possibly attributable to the occurrence of lattice stress in the central pillar region, inhibiting oxygen diffusion, central silicon cores 20 remain in the silicon layer zones 5A'. The silicon cores 20 have a diameter D of only approximately 2 nm, as clearly illustrated in figure 4B.

Even with a layer thickness of 10 nm of the silicon layer zones 5A', a level division of the electronic states with respect to the vertical dimension is achieved. A further reduction in the layer thickness of the silicon layer zones 5A' (and consequently of the

silicon cores 20) to approximately 2 nm allows single-electron components which can be operated at room temperature to be created.

The further process sequence for building up the vertical quantum component or vertical single-electron component which can be produced in this way corresponds substantially to the process steps shown in figures 1L to P. In this case, the oxide sheath layer 13' of the pillar structures 12' can be reduced in its thickness by a suitable etching step before the polysilicon layer 14 is applied ("gate filling"), in order to achieve an even better punchthrough of the gate potential into the active silicon core 20.

Since the lateral, self-restricting oxidation step is likewise a conventional process step, the vertical-quantum or single-electron components can also be produced by using only conventional process steps.

Patent claims

1. A method for producing a vertical semiconductor transistor component, in which
   - a series of layers (5, 6, 7), which comprises layers with different electrical conductivities, is produced over a substrate (1);
   - a random mask with randomly distributed mask structures (9, 10) is formed over the series of layers (5, 6, 7);
   - the random mask is used to form from the series of layers (5, 6, 7) pillar structures (12, 12') which are in electrical connection with one another at the base of the pillars to realize a first electrical contact (K1);
   - isolation layers (13, 13') are produced on the circumferential walls of the pillar structures;
   - an electrically conductive material (14), which realizes a second electrical contact (K2) of the semiconductor transistor component, is deposited between the pillar structures (12, 12') provided with isolation layers (13, 13'); and
   - an electrically conductive bonding material (17.3), which electrically bonds the capping regions of the pillar structures (12, 12') together, is deposited to realize a third electrical contact (K3).

2. The method as claimed in claim 1, characterized
   - in that the series of layers (5, 6, 7) is built up by a selective n^+pn^+ or p^+np^+ epitaxial step.

3. The method as claimed in claim 1, characterized
   - in that the series of layers (5, 6, 7) is built up by a deposition of alternating semiconductor layers and tunnel

isolation layers, the layer thickness of the tunnel isolation layers being less than 5 nm.

4. The method as claimed in claim 3, characterized
   - in that the semiconductor layers consist of silicon, and
   - in that, after the pillar structures (12') have been formed, a lateral, self-restricting oxidation step is executed to produce silicon pillar structure cores (20) of reduced lateral dimensions.

5. The method as claimed in one of the preceding claims, characterized
   - in that the number of pillar structures (12, 12') formed is set by a mask selection step (L2) specifically to a desired value, which lies in particular between 100 and 200.

6. The method as claimed in one of the preceding claims, characterized
   - in that the random mask is produced by chemical vapor deposition (CVD) of a material on a surface over the series of layers (5, 6, 7), which material forms seeds (9, 10) during the deposition on the surface.

7. The method as claimed in one of the preceding claims, characterized
   - in that the random mask is produced by chemical vapor deposition (CVD) of a continuous layer on a surface over the series of layers (5, 6, 7) and a subsequent annealing step to disintegrate the layer into individual seeds (9, 10).

8. A vertical semiconductor transistor component, with vertical pillar structures (12, 12') built up over a substrate (1) by using a random mask,

- which structures are in electrical connection on the base side with a first common electrical contact (K1),
- which structures comprise in the vertical direction layer zones (5A, 6A, 7A; 5A', 6A') of differing conductivity,
- which structures are provided on their circumferential walls with isolation layers (13, 13'), an electrically conductive material (14) which realizes a second electrical contact (K2) of the semiconductor transistor component being deposited between the circumferentially isolated pillar structures (12, 12'), and
- which structures are electrically bonded on the capping side to a third common electrical contact (K3).

9. The vertical semiconductor transistor component as claimed in claim 8, characterized
- in that the pillar structures (12) comprise in the vertical direction a n^+pn^+ or p^+np^+ series of layer zones (5A, 6A, 7A).

10. The vertical semiconductor transistor component as claimed in claim 8, characterized
- in that the pillar structures (12') respectively comprise at least one tunnel isolation layer zone (6A').

11. The vertical semiconductor transistor component as claimed in claim 10, characterized
- in that the pillar structures (12') comprises in the vertical direction a series of layer zones with at least two silicon core layer zones (20, 13'), separated by the tunnel isolation layer zone (6A'), the lateral dimensions (D) of the silicon cores (20) within the silicon core layer zones (20, 13') being less than 20 nm.

12. The vertical semiconductor transistor component as claimed in one of claims 8 to 11, characterized
- in that the component contains between 100 and 200 pillar structures.

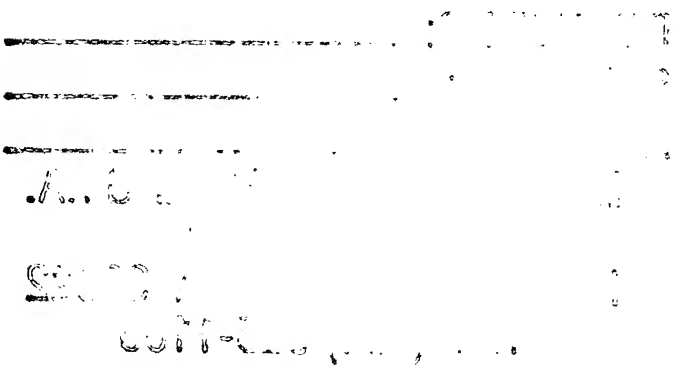
GR 99 P 2315

Abstract

Method for producing a vertical semiconductor transistor component and a vertical semiconductor transistor component

A dual-gate MOSFET semiconductor layer structure is built up on a substrate (1). This structure comprises a first and a second gate electrode (10A, 10B), between which a semiconductor channel layer zone (4A) is embedded, and also a source region (2A) and drain region (2B), which are arranged on opposing faces of the semiconductor channel layer zone (4A). At one of the gate electrodes (10B) there is provided at least one further semiconductor channel layer zone (6A), the faces of which are likewise electrically bonded to the source (2A) and drain regions (2B).

(Figure 1)



A DOCPHOENIX

FOLLOW-ON DOCUMENT INDEX SHEET

INCOMING

_____ ACPA _____
Continuing Prosecution Application

_____ AP.B _____
Appeal Brief

_____ C680 _____
Request for Corrected Notice/Allowance

_____ C.AD _____
Change of Address

_____ CFILE _____
Request for Corrected Filling Receipt

_____ COCIN _____
Papers filed re Certificate of Corrections

_____ CRFD _____
Computer Readable Form Defective

_____ CRFE _____
Computer Readable Form 'ENTERED'

_____ EABN _____
Request for Express Abandonment

_____ ELC. _____
Response to Election/Restriction

_____ IFEE _____
Issue Fee Transmittal PTOL 85 B

_____IRFND_____
Refund Request

_____ L_RIN_____
Any Incoming to L&R

_____ N417 _____
Copy of EFS Receipt Acknowledgement

_____ N/AP _____
Notice of Appeal

_____ PA.. _____
Change in Power of Attorney

_____ PC/I _____
Power to Make Copies or to Inspect

_____ PEF._____
Pre-Exam Formalities Response

_____ PEFRREISS _____
Pre-Exam Formalities Reissue Response

_____PEFRSEQ _____
Pre-Exam Formalities Sequence Reply

INCOMING

_____ LET. _____
Misc. Incoming Letter

_____ IMIS _____
Miscellaneous Internal Document

_____PGEA _____
Req Express Aband to avoid Publication

_____PGA9_____
Req for Corrected Pat App Publication

_____PGREF _____
Req for Refund of Publication Fee Paid

_____PROTEST_____
Protest Documents Filed by 3rd Party

_____PROTRANS_____
Translation of Provisional in Nonprovionl

_____ REM _____
Applicant Remarks in Amendment

_____ RESC _____
Rescind Non-Publication Request

_____ RETMAIL. _____
Mailed Returned by Post Office

_____ XT/ I_____
Extension of Time filed separate

APPL PARTS

_____ 371P _____
PCT Papers in a 371Application

_____ A... _____
Amendment Including Elections

_____ A.NE _____
After Final Amendment

_____ A.PE _____
Preliminary Amendment

_____ ABST _____
Abstract

_____ ADS _____
Application Data Sheet

_____ AF/D _____
Affidavit or Exhibit Received

_____ APPENDIX _____
Appendix

APPL PARTS

_____ ARTIFACT _____
Artifact

_____ CLM _____
Claim

_____ COMPUTER _____
Computer Program Listing

_____ CRFL_____
CRF Transfer Request

_____ CRFS _____
Computer Readable Form Statement

_____ DIST _____
Terminal Disclaimer Filed

_____ DRW _____
Drawings

_____ FOR _____
Foreign Reference

_____ FRPR _____
Foreign Priority Papers

_____ IDS _____
IDS Including 1449

_____ NPL _____
Non-Patent Literature

_____ OATH _____
Oath or Declaration

_____ PET. _____
Petition

__PGPUB DRAWINGS___
Box PG Pub Drawings

_____ SEQLIST _____
Sequence Listing

_____ SPEC _____
Specification

_____ SPEC NO _____
Specification Not in English

6/26/03